Analysis and Design of Radiation-Hardened Phase-Locked Loop(別紙/accompanying paper)

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CITATION:

Kim, Sinnyoung. Analysis and Design of Radiation-Hardened Phase-Locked Loop. 京都大学, 2014, 博士(情報学)

ISSUE DATE:

2014-03-24

URL:

https://doi.org/10.14989/doctor.k18413

別紙

- SinNyoung Kim, Akira Tsuchiya, and Hidetoshi Onodera, “Analysis of Radiation-Induced Clock-Perturbation in Phase-Locked Loop,” *IEICE Transactions on Fundamentals*, to appear, vol.E97-A, no. 3, March 2014. (© 2014 IEICE)
- SinNyoung Kim, Akira Tsuchiya, and Hidetoshi Onodera, “Radiation-Hardened PLL with a Switchable Dual Modular Redundancy Structure,” *IEICE Transactions on Electronics*, to appear, vol. E97-C, no. 4, April 2014. (© 2014 IEICE)
- SinNyoung Kim, Akira Tsuchiya, and Hidetoshi Onodera, “Modeling of Single-Event Failures in Divider and PFD of PLLs based on Jitter Analysis,” *Proceedings of IEEE Conference on RADiation and its Effects on Components and Systems (RADECS)*, PF-3, Sep. 2012. (© 2012 IEEE)
- SinNyoung Kim, Akira Tsuchiya, and Hidetoshi Onodera, “Perturbation-immune radiation-hardened PLL with a switchable DMR structure,” *Proceedings of IEEE 19th International On-Line Testing Symposium (IOLTS)*, pp. 128 - 132, July 2013. (© 2013 IEEE)
- Fujita Tomohiro, SinNyoung Kim, and Hidetoshi Onodera, “Computer Simulation of Radiation-Induced Clock-Perturbation in Phase-Locked Loop with Analog Behavioral Model,” *Proceedings of 15th International Symposium on Quality Electronic Design (ISQED)*, to appear, March 2014. (© 2014 IEEE)

- Figure 4.16: Microphotograph of PLLs designed with 0.18 um CMOS process. (© 2013 IEEE)
- Figure 5.1: Basic concept of proposed RHPLL based on dual modular redundancy (DMR) with detectors. (© 2013 IEEE)
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- Figure 5.9: Full structure of proposed RH-PLL. (© 2013 IEEE)